CLAIMS

Having thus described the invention in detail, what we claim as new and desire to secure by Letters Patent is:

1. A method of forming a thin channel MOSFET comprising:

providing a SOI substrate having an SOI layer located on a buried insulating layer;

forming a block mask having a channel via atop said SOI substrate;

providing a localized oxide region in said SOI layer on top of said buried insulating layer thereby forming a thinned portion of said SOI layer, said localized oxide region being self-aligned with said channel via;

forming a gate in said channel via;

removing at least said block mask; and

forming source/drain extensions in said SOI layer abutting said thinned portion of said SOI layer.

2. The method of Claim 1 wherein providing said localized oxide region further comprises:

implanting oxygen dopant through said channel via to create a dopant profile in a portion of said SOI layer; and

annealing said SOI substrate to convert said dopant profile into said localized oxide region in top of and in contact with said buried insulating layer thereby thinning said portion of said SOI layer.

3. The method of Claim 2 wherein said SOI layer comprises a thickness ranging from about 20.0 nm to about 70.0 nm.

4. The method of Claim 2 wherein said SOI layer further comprises isolation regions.

5. The method of Claim 2 wherein said oxygen dopant is implanted with a dopant concentration ranging from $1x10^{14}$ atoms/cm^2 to $2x10^{18}$ atoms/cm^2.

6. The method of Claim 2 wherein said oxygen dopant is implanted with an implant energy ranging from $1x10^{14}$ atoms/cm^2 to $2x10^{18}$ atoms/cm^2.

7. The method of Claim 2 wherein said oxygen dopant is implanted using an ion implantation apparatus having a current beam density ranging from about 5.0 mA cm^{-2} to about 10.0 mA cm^{-2}.

8. The method of Claim 2 wherein said SOI layer comprises Si, SiGe, SiGeC, SiC or combinations thereof.

9. The method of Claim 2 wherein said localized oxide region thins said portion of said SOI layer to less than about 50.0 nm.

10. The method of Claim 2 further comprising forming a material stack on said SOI substrate prior to forming said block mask, said material stack including a pad oxide layer positioned on said SOI layer and an etch stop layer positioned on said pad oxide layer.

11. The method of Claim 10 wherein said etch stop layer comprises Si_3N_4.

12. The method of Claim 10 wherein said forming said block mask having said channel via further comprises:

forming a dummy gate region atop said material stack;

forming a masking layer substantially coplanar with a top surface of said dummy gate region;

removing said dummy gate region to produce said block mask having said channel via; and

forming a conformal film atop said block mask and within said channel via.

13. The method of Claim 12 wherein said masking layer is a high-density plasma oxide.

14. The method of Claim 10 wherein said etch stop is formed by a deposition process selected from the group consisting of chemical vapor deposition, room temperature chemical vapor deposition, and plasma enhanced chemical vapor deposition and has a thickness ranging from about 50.0 nm to about 150.0 nm.

15. The method of Claim 12 wherein forming said dummy gate region comprises

depositing a layer of polysilicon atop said etch stop layer;

applying a patterned photoresist to said layer of polysilicon; and

etching said regions of said layer of polysilicon not underlying said patterned photoresist to form said dummy gate region.

16. The method of Claim 15 wherein said etching said regions of said layer of polysilicon not underlying said pattered photoresist comprises HBr etch chemistries.

17. The method of Claim 15 further comprising removing said patterned photoresist using an O_2 ash process.

18. The method of Claim 12 wherein said removing said dummy gate region comprises etching said dummy gate regions with bromide gas etch chemistries having a high selectivity to said etch stop layer.

19. The method of Claim 18 wherein said dummy gate region is removed using chemical deposition etching or KOH stopping on said etch stop layer.

20. The method of Claim 12 wherein said forming said gate in said channel via comprises:

etching horizontal surfaces of said conformal film and said material stack to expose said SOI layer;

forming a gate dielectric atop said SOI layer;

forming a gate conductor atop said gate dielectric and

removing said block mask.

21. The method of Claim 20 wherein said gate dielectric is formed by thermal oxidation.

22. The method of Claim 20 wherein said forming said gate conductor comprises blanket depositing a gate conductor material atop said block mask and atop said gate

dielectric and planarizing said gate conductor material until said gate conductor material is coplanar with said block mask.

23. The method of Claim 20 wherein etching said material stack layer comprises:

etching said etch stop layer selective to said pad oxide layer; and

etching said pad oxide layer with a chemical oxide removal process comprising a vapor or plasma of HF and NH_3.

24. The method of Claim 20 where said gate conductor material is polysilicon.

25. The method of Claim 20 wherein said polysilicon is doped prior to said removing said block mask.

26. The method of Claim 1 wherein forming source/drain extension regions further comprises doping said SOI layer with a group IIIA or a group V dopant.

27. The method of Claim 1 wherein said source/drain extension regions have a thickness of about 20.0 nm to about 70.0 nm.

28. A thin channel MOSFET comprising:

a SOI substrate comprising a SOI layer overlying a uniform insulator layer, said SOI layer having a lesser thickness portion and a greater thickness portion;

a gate region atop said SOI substrate having composite spacers;

source and drain extension regions within said greater thickness portion of said SOI layer;

a channel self-aligned to said gate region and separating said source and drain extension regions, said channel located in said lesser thickness region of said SOI layer; and

a localized oxide region atop said uniform insulator layer and underlying said channel region.

29. The thin channel MOSFET of Claim 26 wherein said composite spacer comprises a nitride spacer overlying a pad oxide spacer, where said pad oxide region is positioned in the shadow of the overlying nitride spacer.

30. The thin channel MOSFET of Claim 26 having an external resistance of less than about 400.0 Ohm/μm.